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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE (REV. 7-80) PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use several sheets if necessary)* DATE MAILED: March 7, 2002	ATTY. DOCKET NO. 010544	SERIAL NO. 10/010,199
	APPLICANT Butler, et al.	
	FILING DATE December 4, 2001	GROUP 2133

U.S. PATENT DOCUMENTS

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	A1						
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EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS
	B1						
	B2						
	B3						
	B4						
	B5						
	B6						
	B7						

OTHER PRIOR ART (*Including Author, Title, Date, Pertinent Page, Etc.*)

DG	C1		Rizzo, Luigi., *On the feasibility of software FEC*; Dip. di Ingegneria dell'Informazione, Universita di Pisa, via Diotisalvi 2 – 56126 Pisa (Italy)
	C2		

EXAMINER [signature] DATE CONSIDERED 8/19/2004

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use several sheets if necessary)*	APPLICANT Butler et al.	
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EXAMINER INITIAL	Ref No	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS
DG	B1	0 4 0 7 1 0 1 A2	01/09/91	EP	Digital Equipment Corp.	G11B	20/18
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DG	C1		Katayama,Y et al: "One-Shot Reed-Solomon Decoding For High-Performance Dependable Systems", 2000 IEEE International Networks, NY, USA, June 25, 2000, pages 390-399.
DG	C2		Alzahrani, F et al: "On-Chip TEC-QED ECC For Ultra-Large, Single-Chip Memory Systems", Proceedings IEEE International Conference On Computer Design, October 10, 1994, pages 132-137.
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DG	C4		Nagvajara, P : "Multichip Module Diagnosis, Electro/94 International Conference Proceedings, Boston, MA, IEEE, USA. Combined Volumes, May 10, 1994, pages 793-802.

EXAMINER D Banks	DATE CONSIDERED 8/19/2004

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